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Design of Low-Power Double Tail Dynamic Comparator

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Abstract: In recent years, there has been an increasing demand for high-speed digital circuits at low power consumption. This need for ultra-low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. So in this paper, an analysis on the power of the dynamic comparators will be presented with respect to proposed comparator. All these analysis is done Microwind software.

Keywords:Analog to digital Converter (ADCs), Double Tail Comparator, Voltage swing.

I. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog to digital converters. Many high speed analog to digital converters such as flash analog to digital converter require high speed and low power comparator with small chip area. In electronics field, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals $V+$and $V-$and one binary digital output $V0$. The output is ideally

$V0$ =1, if $V+ > V-$

0, if $V+ < V-$

A comparator consists of specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to digital converters (ADCs)

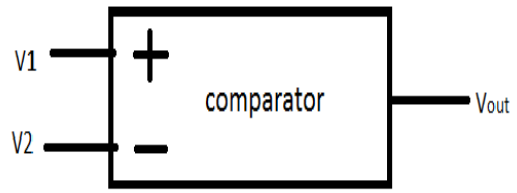

Figure1: Schematic of conventional comparator

Comparator basically compares two voltages or current signals. Figure 1 shows basic operation of comparators where the output is always in digital form, 1 or 0. Apart from technological modifications, developing new circuit structures too avoid stacking of too many transistor between the supply rails is preferable for low voltage operation, without increasing the circuit complexity. Additional circuitry can also be used by adding it to the conventional dynamic comparator to enhance the speed in low supply voltages. Despite this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. Here the structure of double-tail dynamic comparator proposed in this research work is based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. A comprehensive analysis on power of dynamic comparators has been presented for various architectures.

Here, based on the conventional double-tail structure a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Here just by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator. between two inputs) of a modern rail-to-rail comparator is usually limited only by the full swing of power supply.

II. DYNAMIC (CLOCKED REGENARTIVE) COMPARATORS, PROPOSED WORK & SIMULATION RESULT

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback. Recently, many analysis have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset and random decision errors, and kick-back noise.

A. Conventional dynamic comparator

The schematic diagram of the conventional dynamic comparator [1],[2],[13]shown in figure 2(a) which is widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in fig. The operation of the comparator is done in two phase which are as follows: First during the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Out_n and Out_p to VDD to define a start condition and to have a valid logical level during reset and Second in the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Out_p, Out_n), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where $V_{INP} > V_{INN}$, Out_p discharges faster than Out_n, the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back

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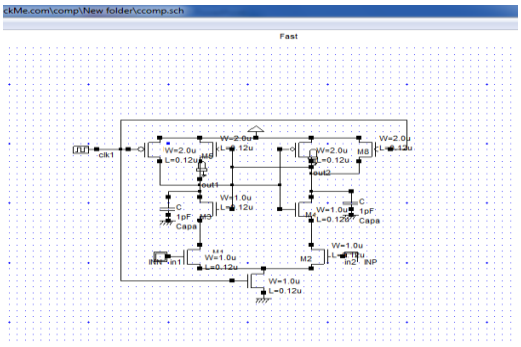
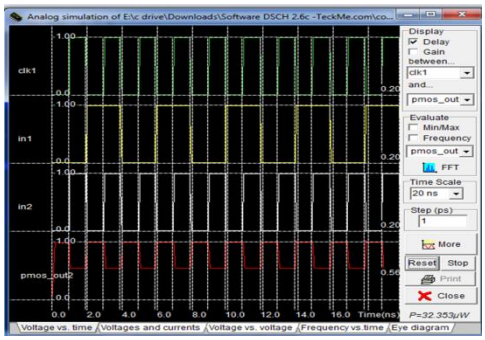
inverters (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Out_p discharges to ground. If VINP < VINN, the circuits works vice versa.

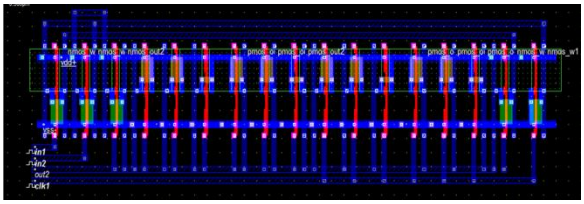
On the basis of schematic diagram its analog simulation and layout diagram shown in figure 2(b-c)



(a)



(b)



(c)

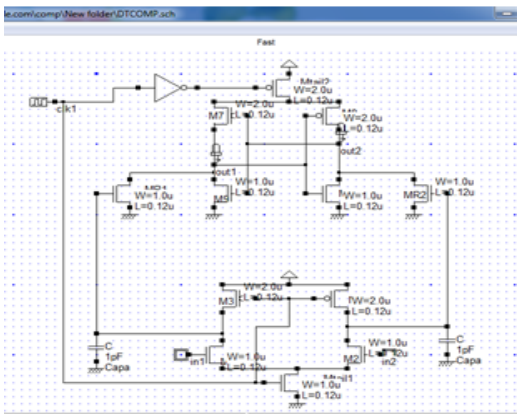
Fig.2(a-c): (a)Schematic (b)Analog Simulation (c)Layout diagram of Conventional Dynamic Comparator

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. But the disadvantage on the other hand, is that due to several stacked transistors, the delay time of the latch becomes large due to lower transconductances. Another important drawback of this structure is that there is only one current path, which is not favourable for regeneration.

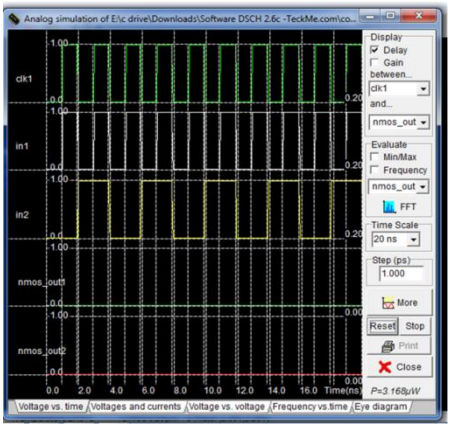
B. Double tail comparators

As there are some disadvantages in conventional dynamic comparator so here we are going to study a conventional double-tail comparator is shown in Figure 3(a) [1], [10]. This topology has less stacking and therefore can operate at lower supply voltages. Here the double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset.

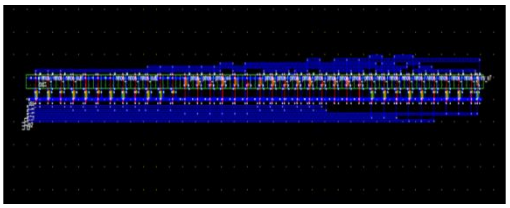
Operation of this comparator as follows:(t_o and t_{latch}) During reset phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground. And then during decision-making phase (CLK = VDD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent Differential voltage ΔVfn(p) will build up. The intermediate stage formed by *M*R1 and *M*R2 passes *V*fn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise. On the basis of schematic diagram its analog simulation and layout diagram shown in figure 3(b-c)



(a)



(b)



(c)

Fig.3(a-c): (a)Schematic (b)Analog Simulation (c)Layout diagram of Conventional Double Tail Comparator

C. Proposed Comparator

The operation of the proposed comparator is as basic conventional double tail dynamic comparator but the thing is that it has two input controlling transistors Mc1 and Mc2 and two transitional stage transistors MR1 and MR2

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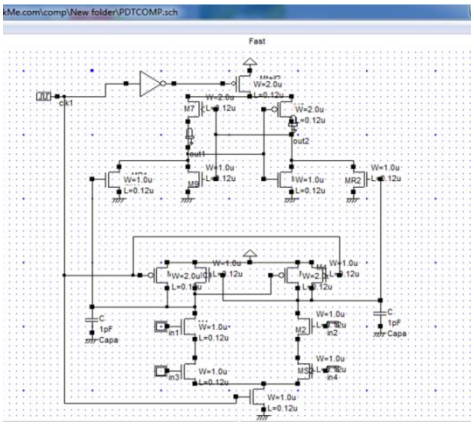
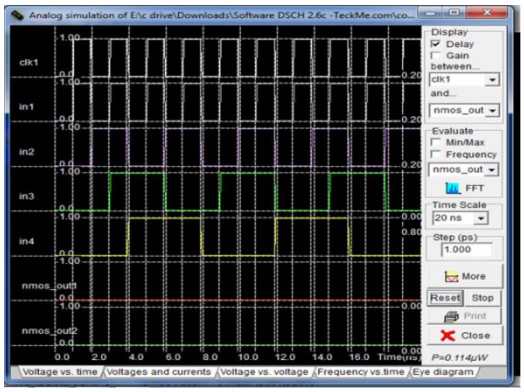
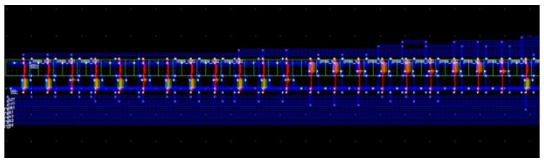
as shown in figure 4(a). It too works in Reset and Transition phase has two timing parameters t_o *and* t_{latch}
On the basis of schematic diagram its analog simulation and layout diagram shown in figure 4(b-c)



(a)



(b)



(c)

Fig 4(a-c): (a)Schematic (b)Analog Simulation (c)Layout diagram of Proposed Double Tail Dynamic Comparator

D. Performance comparison

All schematic design in DSCH in 120nm technology and simulation is done under 90nm technology using Microwind tool.

TABLE I
Performance comparisions

Technique used	Power consumption (µw)	Delay (ps)	Time (ns)
Conventional Dynamic Comparator	32.353	25	20
Double tail Comparator	3.168	20	20
Proposed Dynamic Double tail Comparator	0.114	14	20

Based on this table shown above a graphical presentation is shown in figure 5.

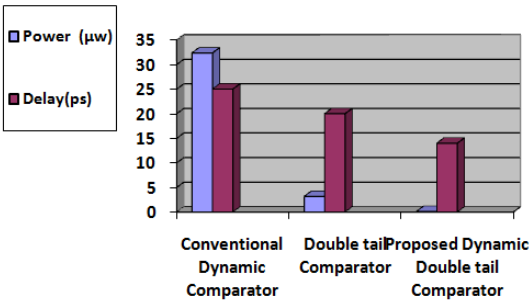


Fig 5: Graphical presentation of delay and power

III. CONCLUSION

In this paper, we presented a comprehensive delay and power analysis for clocked dynamic comparators is done and for that two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were studied and analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator.

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